REMARKS

Claims 1-19 have been presented for examination in the above-identified U.S. Patent Application.

Claims 1-19 have been rejected in Office Action dated April 22, 2004.

Claims 1, 5, 8, 10-13, and 14-17 have been amended by this Amendment A.

Claims 1-19 are still in the Application and reconsideration of the Application is hereby respectfully requested.

Referring to Paragraph 2 on page 2 of the Application, Claims 1,2, 4-6, 10, 11, and 14 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,587,455 issued in the name of Kanuma. Referring to paragraph 11, Claims 3, 7-9, 12, 13, and 15-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Kanuma, cited previously.

Before discussing the rejection of the Claims, the invention of the Application will be summarized. The invention of the Application addresses the relatively recent problem of extending the battery life in portable electronic devices. This extension of the battery life has become increasingly important as the processing power in each device continues to increase. Even the relatively

simple cell phone implements the computational-intensive fast Fourier transform algorithms, Viterbi algorithms, etc. It has become increasingly important to reduce the battery drain as the devices have become further miniaturized. Components that require continuing power are the buses, internal and external. During logic state transitions, the battery provides power to charge and discharge the line capacitors. The present invention provides a technique for measuring the power consumed by a bus during a predetermined operational activity. For example, algorithms can be modified in an effort to reduce the bus activity and thereby lower the power consumption. Thus the present example fills the need for providing a technique to determine whether the modification to the algorithm did, in fact, reduce the power consumption. This technique is performed by determining the power required for each logic state transition and measuring the number of transitions. Thus, the power consumption for a particular algorithm, portion of an algorithm, instruction, processor activity, etc. can be determined.

Returning now to the Kanuma reference, to place this reference in perspective, the filing date was in May, 1984, i.e., twenty years ago. Generally, while battery life in portable electronic apparatus has always been a consideration, at this early date, power consumption was not the critical problem found in modern signal processing units. Specifically, the Kanuma reference does not deal with power consumption, but rather with noise. In the section referenced by Examiner, i.e., Col. 1, lines 39-43, the disclosure makes it clear the principal concern is the current through the power source line, not because of the

power consumption resulting from the current flow, but because charging a multiplicity of bus lines will result in a change in current in the power source line. A large change in current in a single (power source) line at the switching frequencies of the modern computer will result noise radiation. In the individual bus lines these current transitions are not important noise sources; however, in the power source line, the summation of the changes resulting from the summation of the current changes in the individual bus lines can result in problem noise radiation. Examiner appears to equate noise with power. This relationship is more complex. The power source line provides power for the entire processor, not just for the buses. Furthermore, the Kanuma reference is concerned with logic state transitions for each clock cycle and provides no disclosure or teaching of the accumulation on logic state transitions over a plurality of clock cycles.

Comparing the present invention with the Kanuma reference, the Kanuma reference can best be considered as non-analogous art. The Kanuma reference deals with suppression of noise, while the present invention relates to measurement of power consumption. To perform each task, the Kanuma reference and the present invention monitor the transitions on a bus. But each has a different purpose. In the present invention, the number of transitions is measured for a preselected processor operation. The accumulation of logic state transitions is accumulated. The Claims have been amended so that the transitions are measured during selected clock cycles. In this manner, the transition can be measured for portions or all of software programs and for selected processing system operations. In

the Kanuma reference, the number of transitions for each clock cycle is monitored. No accumulation is even hinted at. In addition, the Kanuma reference does not contain any material that would suggest using the apparatus disclosed could be used for power consumption measurements. As pointed out above, the reference to the power source line, involving as it does concern with noise generated over this power source line, would not lead a person of ordinary skill in the art to use similar apparatus for the measurement of power consumption. It appears that Examiner has used the Application as template and interpreted the disclosure of the Kanuma reference in a manner that is not apparent without the hindsight provided by the present Application.

In view of the foregoing discussion, rejection of Claims 1-19 under 35 U.S.C. 102(b) over Kanuma, or in the alternative, rejection of Claims 1-19 under 35 U.S.D.C. 103(a) over Kanuma is respectfully traversed.

CONCLUSIONS

In view of the foregoing discussion and the foregoing amendments, it is believed that Claims 1-19 are now in condition for allowance of and allowance of Claims 1-19 is respectfully requested. Applicant hereby respectfully requests a timely Notice of Allowance be issued in this Application.

Should any issues remain that could be resolved by a telephonic interview, Examiner is requested to telephone the undersigned attorney.

Respectfully submitted,

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